

## ADC0820

# 8-Bit High Speed $\mu$ P Compatible A/D Converter with Track/Hold Function

### General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5  $\mu$ s conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/ $\mu$ s.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

### Key Specifications

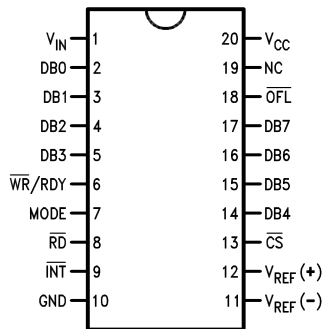
■ Resolution		8 Bits
■ Conversion Time	2.5 $\mu$ s Max (RD Mode)	
	1.5 $\mu$ s Max (WR-RD Mode)	
■ Low Power		75 mW Max
■ Total Unadjusted Error		$\pm 1/2$ LSB and $\pm 1$ LSB

### Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5  $V_{DC}$
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE output
- Logic inputs and outputs meet both MOS and T<sup>2</sup>L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than  $V_{CC}$
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

### Connection and Functional Diagrams

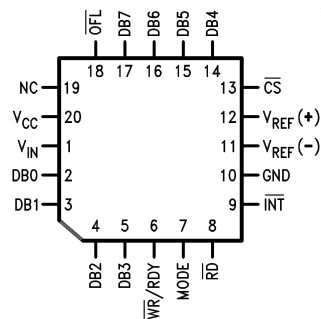
Dual-In-Line, Small Outline and SSOP Packages



Top View

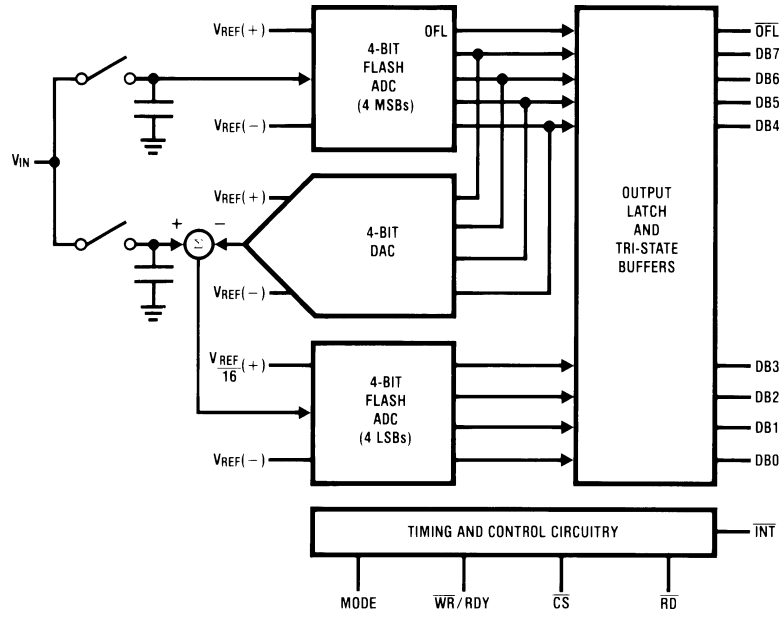
00550101

Molded Chip Carrier Package



00550133

Connection and Functional Diagrams (Continued)



00550102

FIGURE 1.

Ordering Information

Part Number	Total Unadjusted Error	Package	Temperature Range
ADC0820BCV ADC0820BCWM ADC0820BCN	$\pm 1/2$ LSB	V20A—Molded Chip Carrier M20B—Wide Body Small Outline N20A—Molded DIP	0°C to +70°C 0°C to +70°C 0°C to +70°C
ADC0820CCJ ADC0820CCWM ADC0820CIWM ADC0820CCN	$\pm 1$ LSB	J20A—Cerdip M20B—Wide Body Small Outline M20B—Wide Body Small Outline N20A—Molded DIP	-40°C to +85°C 0°C to +70°C -40°C to +85°C 0°C to +70°C

### Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	10V
Logic Control Inputs	-0.2V to $V_{CC} + 0.2V$
Voltage at Other Inputs and Output	-0.2V to $V_{CC} + 0.2V$
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Input Current at Any Pin (Note 5)	1 mA
Package Input Current (Note 5)	4 mA
ESD Susceptibility (Note 9)	900V
Lead Temp. (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C

Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

### Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0820CCJ	-40°C $\leq T_A \leq$ +85°C
ADC0820CIWM	-40°C $\leq T_A \leq$ +85°C
ADC0820BCN, ADC0820CCN	0°C $\leq T_A \leq$ 70°C
ADC0820BCV	0°C $\leq T_A \leq$ 70°C
ADC0820BCWM, ADC0820CCWM	0°C $\leq T_A \leq$ 70°C
$V_{CC}$ Range	4.5V to 8V

### Converter Characteristics

The following specifications apply for RD mode (pin 7=0),  $V_{CC}=5V$ ,  $V_{REF(+)}=5V$ , and  $V_{REF(-)}=GND$  unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A=T_j=25^\circ\text{C}$ .

Parameter	Conditions	ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820BCWM ADC0820CCWM, ADC0820CIWM			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			<b>8</b>			<b>8</b>		Bits
Total Unadjusted Error (Note 3)	ADC0820BCN, BCWM ADC0820CCJ ADC0820CCN, CCWM, CIWM ADC0820CCMSA		<b><math>\pm 1</math></b>			$\pm 1/2$ $\pm 1$ $\pm 1$	<b><math>\pm 1/2</math></b> <b><math>\pm 1</math></b> <b><math>\pm 1</math></b>	LSB LSB LSB LSB
Minimum Reference Resistance		2.3	<b>1.00</b>		2.3	1.2		k $\Omega$
Maximum Reference Resistance		2.3	<b>6</b>		2.3	5.3	<b>6</b>	k $\Omega$
Maximum $V_{REF(+)}$ Input Voltage			<b><math>V_{CC}</math></b>			$V_{CC}$	<b><math>V_{CC}</math></b>	V
Minimum $V_{REF(-)}$ Input Voltage			<b>GND</b>			GND	<b>GND</b>	V
Minimum $V_{REF(+)}$ Input Voltage			<b><math>V_{REF(-)}</math></b>			$V_{REF(-)}$	<b><math>V_{REF(-)}</math></b>	V
Maximum $V_{REF(-)}$ Input Voltage			<b><math>V_{REF(+)}</math></b>			$V_{REF(+)}$	<b><math>V_{REF(+)}</math></b>	V
Maximum $V_{IN}$ Input Voltage			<b><math>V_{CC}+0.1</math></b>			$V_{CC}+0.1$	<b><math>V_{CC}+0.1</math></b>	V
Minimum $V_{IN}$ Input Voltage			<b>GND-0.1</b>			GND-0.1	<b>GND-0.1</b>	V
Maximum Analog Input Leakage Current	$\overline{CS} = V_{CC}$ $V_{IN} = V_{CC}$ $V_{IN} = GND$		<b>3</b> <b>-3</b>			0.3 -0.3	<b>3</b> <b>-3</b>	$\mu\text{A}$ $\mu\text{A}$
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$	$\pm 1/16$	<b><math>\pm 1/4</math></b>		$\pm 1/16$	$\pm 1/4$	<b><math>\pm 1/4</math></b>	LSB

## DC Electrical Characteristics

The following specifications apply for  $V_{CC}=5V$ , unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A=T_J=25^\circ C$ .

Parameter	Conditions		ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820BCWM ADC0820CCWM, ADC0820CIWM			Limit Units	
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)		
$V_{IN(1)}$ , Logical "1" Input Voltage	$V_{CC}=5.25V$	$\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$		<b>2.0</b>			2.0	<b>2.0</b>	V	
		Mode		<b>3.5</b>			3.5	<b>3.5</b>	V	
$V_{IN(0)}$ , Logical "0" Input Voltage	$V_{CC}=4.75V$	$\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$		<b>0.8</b>			0.8	<b>0.8</b>	V	
		Mode		<b>1.5</b>			1.5	<b>1.5</b>	V	
$I_{IN(1)}$ , Logical "1" Input Current	$V_{IN(1)}=5V$ ; $\overline{CS}$ , $\overline{RD}$		0.005	<b>1</b>		0.005		<b>1</b>	$\mu A$	
		$V_{IN(1)}=5V$ ; $\overline{WR}$		0.1	<b>3</b>		0.1	0.3	<b>3</b>	$\mu A$
		$V_{IN(1)}=5V$ ; Mode		50	<b>200</b>		50	170	<b>200</b>	$\mu A$
$I_{IN(0)}$ , Logical "0" Input Current	$V_{IN(0)}=0V$ ; $\overline{CS}$ , $\overline{RD}$ , $\overline{WR}$ , Mode		-0.005	<b>-1</b>		-0.005		<b>-1</b>	$\mu A$	
$V_{OUT(1)}$ , Logical "1" Output Voltage	$V_{CC}=4.75V$ , $I_{OUT}=-360 \mu A$ ; $DB0-DB7$ , $\overline{OFL}$ , $\overline{INT}$			<b>2.4</b>			2.8	<b>2.4</b>	V	
		$V_{CC}=4.75V$ , $I_{OUT}=-10 \mu A$ ; $DB0-DB7$ , $\overline{OFL}$ , $\overline{INT}$			<b>4.5</b>			4.6	<b>4.5</b>	V
$V_{OUT(0)}$ , Logical "0" Output Voltage	$V_{CC}=4.75V$ , $I_{OUT}=1.6 mA$ ; $DB0-DB7$ , $\overline{OFL}$ , $\overline{INT}$ , $RDY$			<b>0.4</b>			0.34	<b>0.4</b>	V	
$I_{OUT}$ , TRI-STATE Output Current	$V_{OUT}=5V$ ; $DB0-DB7$ , $RDY$ $V_{OUT}=0V$ ; $DB0-DB7$ , $RDY$		0.1	<b>3</b>		0.1	0.3	<b>3</b>	$\mu A$	
			-0.1	<b>-3</b>		-0.1	-0.3	<b>-3</b>	$\mu A$	
$I_{SOURCE}$ , Output Source Current	$V_{OUT}=0V$ ; $DB0-DB7$ , $\overline{OFL}$ , $\overline{INT}$		-12	<b>-6</b>		-12	-7.2	<b>-6</b>	mA	
			-9	<b>-4.0</b>		-9	-5.3	<b>-4.0</b>	mA	
$I_{SINK}$ , Output Sink Current	$V_{OUT}=5V$ ; $DB0-DB7$ , $\overline{OFL}$ , $\overline{INT}$ , $RDY$		14	<b>7</b>		14	8.4	<b>7</b>	mA	
$I_{CC}$ , Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$		7.5	<b>15</b>		7.5	13	<b>15</b>	mA	

## AC Electrical Characteristics

The following specifications apply for  $V_{CC}=5V$ ,  $t_r=t_f=20 ns$ ,  $V_{REF(+)}=5V$ ,  $V_{REF(-)}=0V$  and  $T_A=25^\circ C$  unless otherwise specified.

Parameter	Conditions		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$t_{CRD}$ , Conversion Time for RD Mode	Pin 7 = 0, <i>Figure 2</i>		1.6		2.5	$\mu s$
$t_{ACC0}$ , Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Pin 7 = 0, <i>Figure 2</i>			$t_{CRD}+20$	$t_{CRD}+50$	ns
$t_{CWR-RD}$ , Conversion Time for WR-RD Mode	Pin 7 = $V_{CC}$ ; $t_{WR} = 600 ns$ , $t_{RD}=600 ns$ ; <i>Figures 3, 4</i>				1.52	$\mu s$
$t_{WR}$ , Write Time	Min	Pin 7 = $V_{CC}$ ; <i>Figures 3, 4</i>		600		ns
	Max	(Note 4) See Graph	50			$\mu s$
$t_{RD}$ , Read Time	Min	Pin 7 = $V_{CC}$ ; <i>Figures 3, 4</i> (Note 4) See Graph		600		ns
$t_{ACC1}$ , Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Pin 7 = $V_{CC}$ , $t_{RD} < t_r$ ; <i>Figure 3</i>					
	$C_L=15 pF$		190		280	ns
$C_L=100 pF$			210		320	ns

## AC Electrical Characteristics (Continued)

The following specifications apply for  $V_{CC}=5V$ ,  $t_r=t_f=20$  ns,  $V_{REF(+)}=5V$ ,  $V_{REF(-)}=0V$  and  $T_A=25^\circ C$  unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$t_{ACC2}$ , Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Pin 7 = $V_{CC}$ , $t_{RD} > t_i$ ; <i>Figure 4</i> $C_L=15$ pF	70		120	ns
	$C_L=100$ pF	90		150	ns
$t_{ACC3}$ , Access Time (Delay from Rising Edge of RDY to Output Valid)	$R_{PULLUP} = 1k$ and $C_L = 15$ pF	30			ns
$t_i$ , Internal Comparison Time	Pin 7= $V_{CC}$ ; <i>Figures 4, 5</i> $C_L=50$ pF	800		1300	ns
$t_{1H}$ , $t_{0H}$ , TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L=1k$ , $C_L=10$ pF	100		200	ns
$t_{INTL}$ , Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = $V_{CC}$ , $C_L= 50$ pF $t_{RD} > t_i$ ; <i>Figure 4</i> $t_{RD} < t_i$ ; <i>Figure 3</i>			$t_i$	ns
		$t_{RD}+200$		$t_{RD}+290$	ns
$t_{INTH}$ , Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	<i>Figures 2, 3, 4</i> $C_L=50$ pF	125		225	ns
$t_{INTHWR}$ , Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	<i>Figure 5</i> , $C_L=50$ pF	175		270	ns
$t_{RDY}$ , Delay from $\overline{CS}$ to RDY	<i>Figure 2</i> , $C_L=50$ pF, Pin 7 =0	50		100	ns
$t_{ID}$ , Delay from $\overline{INT}$ to Output Valid	<i>Figure 5</i>	20		50	ns
$t_{RI}$ , Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7= $V_{CC}$ , $t_{RD} < t_i$ <i>Figure 3</i>	200		290	ns
$t_P$ , Delay from End of Conversion to Next Conversion	<i>Figures 2, 3, 4, 5</i> (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/ $\mu$ s
$C_{VIN}$ , Analog Input Capacitance		45			pF
$C_{OUT}$ , Logic Output Capacitance		5			pF
$C_{IN}$ , Logic Input Capacitance		5			pF

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to the GND pin, unless otherwise specified.

**Note 3:** Total unadjusted error includes offset, full-scale, and linearity errors.

**Note 4:** Accuracy may degrade if  $t_{WR}$  or  $t_{RD}$  is shorter than the minimum value specified. See Accuracy vs.  $t_{WR}$  and Accuracy vs.  $t_{RD}$  graphs.

**Note 5:** When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supply rails ( $V_{IN} < V^-$  or  $V_{IN} > V^+$ ) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

**Note 6:** Typicals are at  $25^\circ C$  and represent most likely parametric norm.

**Note 7:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 8:** Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

**Note 9:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.